Analog to Digital – Analog to Digital (A/D) modules translate analog electrical signals for data processing purposes. NAI offers nine A/D smart function modules. The Adx smart function modules provide fast, accurate and reliable conversion performance ideally suited for military, industrial, and commercial applications. A variety of A/D converters with available channels, architecture type and sampling rates are available to meet your circuit design needs.

Specifications AD1 – AD3

- Resolution: 24-bit Sigma-Delta A/D converters. One per channel
- Input Format: Differential voltage (may be used as single-ended by grounding one input)
- Input Scaling: Twelve (12) bipolar or unipolar channels (volts). Programmable, per channel, as Full Scale (FS) range inputs of ± 25 mA where range is -FS to +FS or 0 to FS mA. The ability to set lower currents for FS assures the utilization of the full resolution.
- Overvoltage Protection: No damage up to ±12 V continuous; ±30 V momentary
- Open Input Sense: This module will NOT sense and report unconnected inputs.
- Input Impedance: 50 Ω min.
- Linearity/Accuracy: ±0.1% FS range over temperature (current), to 16-bits
- Gain Error: ±0.1% (current)
- Offset Error: ±0.2% FS range
- Sampling Rate: 256 kHz max per channel, programmable
- Data Buffering/Triggering: See Operations Manual for details.
- Bandwidth: 20 kHz per channel
- Group Delay: 144 µs (based on 250 kHz sampling rate) (time for data sample to propagate to data register)
- Programmable Filter: Each channel incorporates an anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 128 kHz in 1 Hz steps).
- Common Mode Rejection: 70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 kHz.
- Common Mode Voltage: Signal voltage plus Common mode voltage is 10.5 volts. Note: A/D differential inputs must not "float". Input source must have return path to ground.
- Output Logic: Bipolar output in two's complement. Bipolar output range from FF80 0000 max. negative; 007F FFFF max. positive (FS) Unipolar output range from 0 to 00FF FFFF (FS)
- ESD Protection: Designed to meet the testing requirements of IEC 801-2 Level 2 (4 KV transient with a peak current of 7.5 A and Tc of approximately 60 ns).
- Power: 5 VDC @ 750 mA max.
- Ground: Channel inputs are differential, referenced to isolated module AGND, isolated (250 V minimum peak isolation) from system power/ground.
- Weight: 1.5 oz. (42 g)
- VREF Detail: VREF output @ 4.096 V (≤ 10 mA)

AD4

- Resolution: 16-bit SAR A/D converters. One per 8 channel multiplexed bank / 2 banks.
- Input Format: Differential voltage (may be used as single-ended by grounding one input). Single direction DC current.
- Input Scaling: Sixteen (16) bipolar or unipolar channels (volts) or unipolar (current). Programmable, per channel, as Full Scale (FS) range inputs of 10.00, 5.00, 2.50 or 1.25 volts where range is -FS to +FS, 0 to FS VDC, or ±25 mA. The ability to set lower voltages for FS assures the utilization of the full resolution.
- Overvoltage Protection: No damage up to ±12 V continuous; ±30 V momentary
- Overcurrent Protection: 30 mA (When AD4 is set for current mode.)

- Open Input Sense: This module will sense and report unconnected inputs.
- Input Impedance: 10 MΩ min. / or 49.9 Ω current mode; 20 MΩ (Differential)
- Linearity/Accuracy: ±1.25 V or 0 to 1.25 V Range: ±0.1% + (±25 mV) All Other Ranges: ±0.1% FS range over temperature (voltage/current), no missing codes to 16-bits
- Gain Error: ±0.1% FS range (voltage mode) ±0.25% FS range (current mode)
- Offset Error: ±0.04% FS range or ±5 mV, the greater of (voltage mode) ±0.02% FS range (current mode)
- Integral Non-Linearity (INL): ±3 LSB's max.
- Differential Non-Linearity (DNL): ±1 LSB's max. (monotonic)
- Sampling Rate: 400 KSPS maximum aggregate, per bank of 8 channels, programmable. 500 KSPS pending.
- Data Buffering/Triggering: Programmable channel sampling scan (programmable for all (16) channels). Each channel per bank can be programmed for selective scanning sequence. See Operations Manual for details.
- Acquisition/Conversion Time: 3 µs / with filter – single channel scan.
- Throughput: 3 µs max. (between samples - time for data sample to propagate to data register) / with filter – single channel scan.
- Programmable Filter: Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 200 kHz in 10 Hz steps).
- Common Mode Rejection: 90 dB min. at 60 Hz. Roll off to 50 dB min. at 10 kHz.
- Common Mode Voltage: Signal voltage plus Common mode voltage is 10.5 volts. Note: A/D differential inputs must not "float". Input source must have return path to ground.
- Output Logic: Bipolar output in two's complement Bipolar output range from FFFF 8000 max. negative; 0000 7FFF is max. positive (FS) Unipolar output range from 0 to 0000 FFFF (FS) (Voltage Ranges only)
- ESD Protection: Designed to meet the testing requirements of IEC 801-2 Level 2. (4 kV transient with a peak current of 7.5 A and a Tc of approximately 60 ns)
- Power: 5 VDC @ 100 mA or 150 mA max (typ. / max.); +12 VDC @ 220 mA or 330 mA (typ. / max.)
- Ground: Channel inputs are differential, referenced to isolated module AGND (or Common Mode Reference Point (CMRP) – Ch.16(-)) isolated (250 V minimum peak isolation) from system power/ground.
- Weight: 1.5 oz. (42 g)

AD5

- Resolution: 16-bit SAR A/D converters. One per 8 channel multiplexed bank / 2 banks.
- Input Format: Differential voltage (may be used as single ended by grounding one input).
- Input Scaling: Sixteen (16) bipolar or unipolar channels (volts). Programmable, per channel, as Full Scale (FS) range inputs of 50.00, 25.00, 12.50 or 6.25 volts, where range is -FS to +FS or 0 to FS VDC. The ability to set lower voltages for FS assures the utilization of the full resolution.
- Overvoltage Protection: No damage up to ±60 V continuous; ±80 V momentary
- Open Input Sense: This module will NOT sense and report unconnected inputs.
- Input Impedance: 138 kΩ min.; 276 kΩ (Differential)

AD6

- Resolution: 16-bit SAR A/D converters. One per 8 channel multiplexed bank / 2 banks.
- Input Format: Differential voltage (may be used as single-ended by grounding one input).
- Input Scaling: Sixteen (16) bipolar or unipolar channels (volts). Programmable, per channel, as Full Scale (FS) range inputs of 100.00, 50.00, 25.00 or 12.50 volts where range is -FS to +FS or 0 to FS VDC. The ability to set lower voltages for FS assures the utilization of the full resolution.
- Overvoltage Protection: No damage up to ±120 V continuous; ±150 V momentary.
- Open Input Sense: This module will NOT sense and report unconnected inputs.
- Input Impedance: 263 kΩ min.; 526 kΩ

ADE

- Resolution: 16-bit SAR A/D converters. Simultaneous sampling.
- Input Format: Differential voltage (may be used as single-ended by grounding one input).
- Input Scaling: Sixteen (16) bipolar or unipolar channels (volts) or (current). Programmable, per channel, as Full Scale (FS) range inputs where range is -FS to +FS or 0 to FS; 10.00, 5.00, 2.50, 1.25 or 0.625 volts. The ability to set lower voltages for FS assures the utilization of the full resolution.
- Overvoltage Protection: No damage up to 30 V continuous, 36 V momentary
- Open Input Sense: This module will sense and report unconnected inputs.
- Input Impedance: 10 MΩ min. / 20 MΩ (Differential)
- Linearity/Accuracy: ≤ ±1.25 V or 0 to 1.25 V Ranges: ±0.12% + (±25 mV) All Other Ranges: ±0.1% FS range over temperature (voltage/current), no missing codes to 16-bits.
- Gain Error: ±0.1% FS range
- Offset Error: Greater of ±0.04% FS range or ±5 mV
- Integral Non-Linearity (INL): ±3 LSB's max.
- Differential Non-Linearity (DNL): ±1 LSB's max. (monotonic)
- Sampling Rate (Programmable): 200 kSPS maximum (decimation at slower sample rate (< 100 kHz, 1 kHz minimum)
- Data Buffering/Triggering: Independent FIFO sample capture with programmable options (1M 32-bit data elements per channel). See Operations Manual for details.
- Acquisition/Conversion Time: To be characterized
- Programmable Filter: IIR Filter Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable -3 dB break point (programmable from 10 Hz to 90 kHz in 10 Hz steps).
- Common Mode Rejection: 90 dB min. at 60 Hz. Roll off to 50 dB min. at 10 kHz.
- Common Mode Voltage: Signal voltage plus Common mode voltage is 10.5 volts. Note: A/D differential inputs must not “float”. Input source must have return path to A/D Return (CH 16-).
- Output Logic: Bipolar output in two's complement. Bipolar output range from FFFF 8000 max. negative; 0000 7FFF is max. positive (FS) Unipolar output range from 0 to 0000 FFFF (FS) (Voltage Ranges only)
- ESD Protection: Designed to meet the testing requirements of IEC 801-2 Level 2. (4 KV transient with a peak current of 7.5 A and a Tc of approximately 60 ns).
- Power: 5 VDC @ 100 mA /150 mA max. (typ. / max.); ±12 VDC @ 220 mA / 330 mA (typ. / max.)
- Ground: Channel inputs are differential, referenced to isolated module AGND, (or Common Mode Reference Point (CMRP): CH16(-)) isolated (250 V minimum peak isolation) from system power/ground.
- Weight: 1.5 oz. (42 g)

ADF

- Resolution: 16-bit SAR A/D converters. Simultaneous sampling.
- Input Format: Differential voltage (may be used as single-ended by grounding one input).
- Input Scaling: Sixteen (16) bipolar or unipolar channels (volts) or (current). Programmable, per channel, as Full Scale (FS) range inputs where range is -FS to +FS or 0 to FS; 100.00, 50.00, 25.0, 12.5 or 6.25 volts. The ability to set lower voltages for FS assures the utilization of the full resolution.
- Overvoltage Protection: 120 V continuous, 150 V momentary
- Input Impedance: 190 kΩ min. / 380 kΩ (Differential)

ADG

- Resolution: 16-bit SAR A/D converters. Simultaneous sampling.
- Input Format: Current (unipolar and bipolar).
- Input Scaling: Sixteen (16) bipolar or unipolar channels (volts) or (current). Programmable, per channel, as Full Scale (FS) range inputs where range is -FS to +FS or 0 to FS; 25, 12.5 mA. The ability to set lower voltages for FS assures the utilization of the full resolution.

Module	Description
AD1	12 A/D Channels (±1.25 to ±10.0 VDC FSR); 24-bit Sigma-Delta
AD2	12 A/D Channels (±100V max); 24-bit Sigma-Delta
AD3	12 A/D Channels (±25mA FSR); 24-bit Sigma-Delta
AD4	16 A/D Channels (±1.25 to ±10.0 VDC FSR or ±25 mA) ; 16-bit SAR, 8 Chx2 A/D multiplexed
AD5	16 A/D Channels (±6.25 to ±50.0 VDC FS); 16-bit SAR, 8 Chx2 A/D multiplexed
AD6	16 A/D Channels (12.5 to 100.0 VDC FS); 16-bit SAR, 8 Chx2 A/D multiplexed
ADE	16 A/D Channels (±10 VDC); 16-bit SAR per channel
ADF	16 A/D Channels (±100 VDC); 16-bit SAR per channel
ADG	16 A/D Channels (±25 mA); 16-bit SAR per channel

Modules ADE, ADF and ADG feature 16 channels with 16-bit, individual Successive Approximation Register (SAR) A/D converters for each channel. The maximum programmable, expected full-scale range input for the three modules is ±10 V, ±100 V, and ±25 mA, respectively. The A/D converters have programmable sample rates of up to 200 kSPS max per channel.

Modules ADE, ADF and ADG offer advantages including simultaneous sampling, low power and provide field programmable input range and gain for each channel. All A/D channels are 'self-aligning' with Continuous Background Built-in-Test (CBIT), Initiated BIT (IBIT) and extended off-line diagnostics and status provided for channel health and operation feedback. Each channel includes a fixed, second-order, anti-aliasing input filter and a digital, second-order IIR low-pass output filter with a programmable break frequency that enables users to field-adjust the filtering for each channel. The modules also include extended A/D FIFO buffering capabilities for greater storage/management of the incoming signal samples (data) for post processing applications. Programmable FIFO buffer thresholds maximize data flow control (in and out of the FIFO).

Taking advantage of the fast and simultaneous sampling SAR A/D architecture, the module provides an effective A/D interface for applications requiring control loop integration and parallel data acquisition. The A/D Module Threshold, Saturation and Measurement registers can be programmed to be utilized as an IEEE 754 single-precision floating-point value or as a 32-bit integer value. Applications include control loops, data acquisition, synchronous data across channels and additional Programming (thresholds, floating point, etc.)

"The addition of ADE, ADF and ADG smart modules expands our COSA® Architecture aligning with MOSA, SOSA and FACE." states Lino Massafra, VP of Sales and Marketing. "These new modules expand the flexibility, adaptability and modularity offered by our portfolio of board and system level products."

Features

- The input range is field programmable for each channel.
- Each channel includes an anti-aliasing filter and a low-pass filter with a programmable breakpoint.
- All channels have continuous background Built-In-Test (BIT).
- The module(s) also include extended A/D FIFO buffering capabilities for greater storage/management of the incoming samples for post processing applications

Built-In Test (BIT)/Diagnostic Capability

Three different tests, one online (D2) and two off-line (D0, D3), can be selected:
The online (D2) test initiates automatic background BIT testing, where each channel is checked to a test accuracy of 0.2% FS. Any failure triggers an Interrupt (if enabled) with the results available in BIT status register. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus. In addition, all channels are monitored for open input.

The off-line (D3) test starts an initiated BIT test that disconnects all A/D's from the I/O and then connects them across an internal stimulus. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 20 seconds and results can be read from the Status registers when D3 changes from 1 to 0. The test can be stopped at any time and

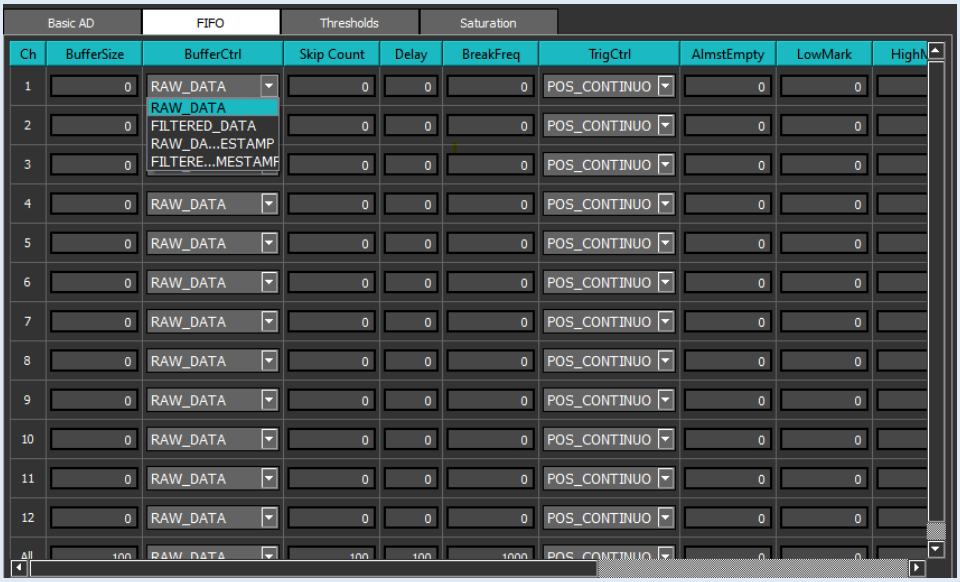
requires no user programming. It can be enabled or disabled via the bus. A/D Open Circuit monitoring is disabled during D3 testing.

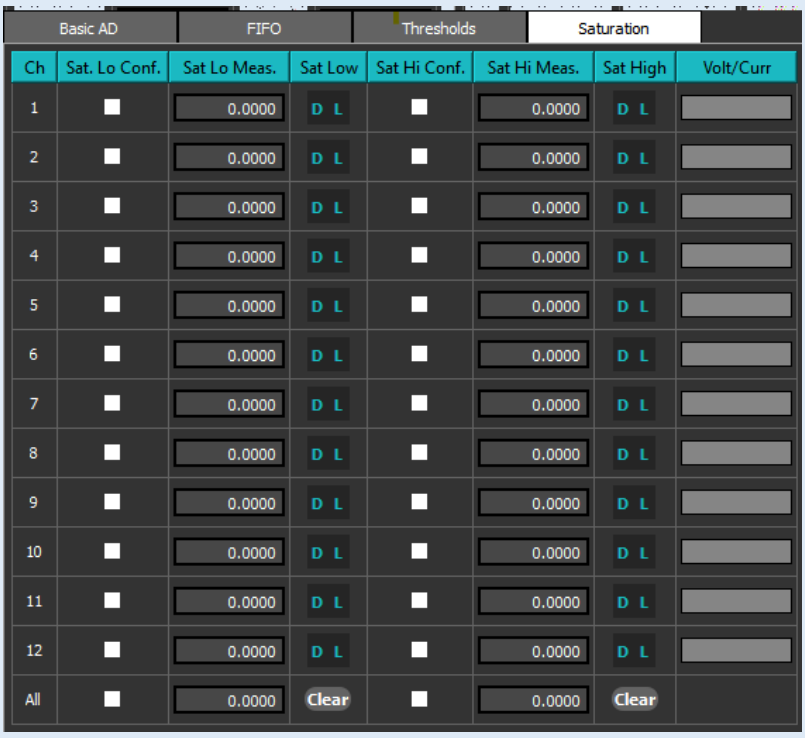
An off-line (D0) test is used to check the card and interface. Write 1 to D0 of Test Enable register to disconnect all A/D channels from the I/O and to connect them across an internal D/A. Test parameters are controlled by the user and are entered in the D0 Test Voltage and D0 Test Range registers. The outputs from the A/D channels are compared to the internal D/A for proper conversion. External reference voltage is not required.

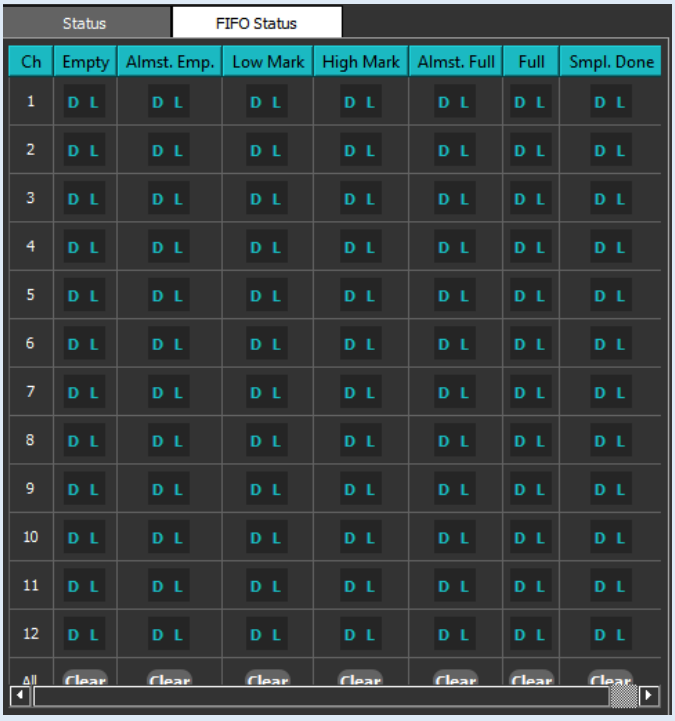
New Embedded Soft Panel

North Atlantic Industries offers the newest cross platform (Windows and Linux) GUI for our Gen 5 products that allows a user to quickly interact with our broad range of modular, I/O cards and rugged embedded computing products. Embedded Soft Panel 2 (ESP 2) is coherent and easy to use with a clean, fleshed out UI with features such as drag and drop dock able windows, a dark and light theme, and multi-language support. Multiple ways to open a board are offered, including saving board opening settings for future use. Interacting with and collecting information on hardware is simple to do with the register editor for reading and writing specific addresses, and the API logger which logs all API library calls including their return status and parameters. ESP 2 has many new features and provides an organized and effortless interface for NAI's next generation products. Available for CentOS 7.4 and 8.2 and Windows 10 x64

A/D Example - Module AD1 Demo Mode Screen Shots







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