









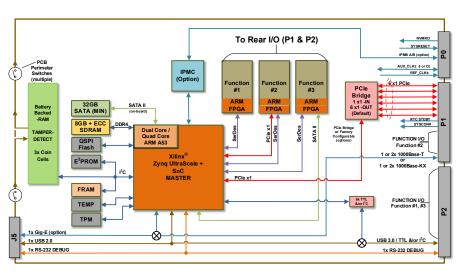
68ARM2 3U OpenVPX™ SBC with Three Smart I/O Function Module Slots

Over 70 different functions to choose from

Configure to Customize

The 68ARM2 is a 3U OpenVPX Zyng® UltraScale+™ Quad-core ARM® Cortex™-A53 MPCore™ based Single Board Computer that can be configured with up to three NAI Smart I/O and communications function modules. Ideally suited for rugged Mil-Aero applications, the 68ARM2 delivers off-the-shelf solutions that accelerate deployment of SWaP-optimized systems in air, land and sea applications.





Features Summary

3U OpenVPX (ANSI/VITA 65)

Profiles Supported:

- MOD3-PAY-1F2U-16.2.11-2
 - Data plane: 6 x1 PCIe (default) (other factory configurations avail.)
 - Control plane: 2x 10/100/1000Base-T or 2x 1000Base-KX
- SLT3-PAY-1F2U-14.2.12

Processor/Memory

- Xilinx Zvng® UltraScale+™ Quad-core ARM® Cortex™-A53 MPCore™ up to 1.3 GHz
- 8 GB DDR4 SDRAM w/ ECC
- 32 GB SATA II NAND Flash

Smart I/O Functions

- Support for 3 independent modules
- PCIe interface to function slot #2 (e.g. for 2 additional Gig-E ports option)
- SATA II interface to function slot #3 (e.g. for 256 GB expansion option)

Security / Cybersecurity (Option)

- FIPS 140-3 Level 3 Design Support
- Crypto-key storage
- Battery-backed RAM
- Secure Boot
- Anti-tamper / Tamper Detect & Sanitize

Motherboard Peripheral I/O:

- USB 2.0 to front maintenance J5 (option)
- USB 3.0 to rear I/O (option)
- I²C Bus to rear I/O (option)
- 1x RS232 console port
 - To front maintenance J5 & rear I/O
- 2x TTL I/O to rear I/O (8x TTL option)

IPMC Support

- VITA 46.11 Tier-2, basic, compatible (configured option)

< 15 W power dissipation (est./tvp.) (not including module power)

Operating Systems

- Xilinx PetaLinux
- Wind River® VxWorks®
- DDC-I Deos

Background Built-in-Test Continuous BIT (as applicable)

- COSA® Architecture
- Intelligent I/O library support (included)
- **VICTORY Interface Services** (Contact factory)
- **Commercial or Rugged Applications**

Operating Temperature

- Commercial: 0°C to 70°C Rugged: -40°C to 85°C

Mechanical Options (ANSI/VITA 48)

- Air-cooled; 3U, 5HP/1.0" pitch
- Conduction-cooled; 3U, 1.0" pitch

68ARM2 Data Sheet Rev. A1 110 Wilbur Place, Bohemia NY 11716 Tel: 631.567.1100 www.naii.com



68ARM2 3U OpenVPX SBC

Select up to 3 functions for your application

For a full listing of available smart functions and detailed specifications please visit https://www.naii.com/functions

| | | Analo | og & | Digital I/O | | |
|---------------------------|-----------|--|-------------|----------------------------------|-----------|--|
| Function | Module | Description | | Function | Module | Description |
| A/D Converter | AD1 | 12 Ch. ±1.25 to ±10.0 VDC FSR; 256 kHz (max), 24-bit Sigma-Delta | | D/A Converter | DA1 | 12 Ch. ±10 VDC or ± 25 mA / Ch. |
| | AD2 | 12 Ch. ±12.5 to ±100.0 VDC FSR; 256 kHz (max), 24-bit Sigma-Delta | | | DA2 | 16 Ch. ±10 VDC @ 10 mA max. / Ch. |
| | AD3 | 12 Ch. ±25 mA FSR; 24-bit 256 kHz (max), Sigma-Delta | | | DA3 | 4 Ch. ±40 VDC or ± 100 mA / Ch. |
| | AD4 | 16 Ch. ±1.25 to ±10.0 VDC FSR or ±25 mA; | | | DA4 | 4 Ch. ±20 to ± 80 VDC @ ±10 mA max. / Ch. |
| | | 16-bit SAR, 8 Ch. x 2 A/D multiplexed, 400 kHZ (aggregate per A/D) | | | | |
| | AD5 | 16 Ch. ±6.25 to ±50.0 VDC FSR; | | | DA5 | 2 Ch. 65 VDC @ ±2 A max., external applied VCC source |
| | | 16-bit SAR, 8 Ch. x 2 A/D multiplexed, 400 kHZ (aggregate per A/D) | | | | |
| | AD6 | 16 Ch. ±12.5 to ±100.0 VDC FSR; | | | DT1 | 24 Ch. Discrete I/O, 0 - 60 VDC, 500 mA / Ch. max. |
| | | 16-bit SAR, 8 Ch. x 2 A/D multiplexed, 400 kHZ (aggregate per A/D) | | | | |
| | ADE | 16 Ch. ±10 VDC FSR; 200 kHz (max.), 16-bit SAR | | | DT2 | 16 Ch. Discrete switch, ±80 V, 625 mA / Ch. max., isolated |
| | ADF | 16 Ch. ±100 VDC FSR; 200 kHz (max.), 16-bit SAR | _ | I/O Discrete | DT3 | 4 Ch. Discrete-switch, 65 V, 2 A / Ch. as half-bridge configuration, ext. VCC or 2 Ch. ±65 V, 2 A / Ch. as full-bridge configuration, ext. VCC |
| | ADG | 16 Ch. ±25 mA FSR; 200 kHz (max.), 16-bit SAR | | | DT4 | 24 Ch. Discrete I/O, 0 - 60 VDC, 500 mA / Ch. max., enhanced operation |
| | | | | | DT5 | 16 Ch. Discrete switch, ±80 V, 625 mA / Ch., enhanced operation |
| I/O TTL/CMOS | | | | | - | 4 Ch. Discrete-switch, 65 V, 2 A / Ch. as half-bridge configuration, ext. VCC |
| | TL1 | 24 Ch. 3.3V/5V tolerant, high-speed, programmable | | | DT6 | or 2 Ch. ±65 V, 2 A / Ch. as full-bridge configuration, ext. VCC |
| | | | | | | (DT3-type enhanced operation TBD/pending) |
| | TL2 | 24 Ch. 3.3V/5V tolerant, high-speed, programmable, enhanced | - - - | I/O Relay | | ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,, |
| | TL3 – TL8 | 24. Ch. 3.3V/5V tolerant, multiple strapping options | | | RY1 | 4 Ch. SPDT, 220 VDC/ 250 VAC, 2 A, 60 W/62.5 VA max., non-latching |
| I/O Differential | DF1 | 16 Ch. RS-422/485 I/O transceiver | | | RY2 | 4 Ch. SPDT, 220 VDC/ 250 VAC, 2 A, 60 W/62.5 VA max., latching |
| | DF2 | 16 Ch. RS-422/485 I/O transceiver, enhanced | | | | |
| | | Position, Timing, I | Mea | surement & Simul | ation | |
| Function | Module | Description | | Function | Module | Description |
| AC Reference | AC1 | 1 Ch. 2-28 Vrms (LV) & 1 Ch. 28-115 Vrms (HV), programmable | - - - | SYN/RSL-to-Dig | SD1 | 4 Ch. 2-28 Vrms Input, 2-115 Vrms Exc, 47 Hz - 1 Hz Freq |
| | AC2 | 2 Ch. 2-28 Vrms (LV), 47 Hz -20 kHz (max. range), | | | SD2 | 4 Ch. 2-28 Vrms Input, 2-115 Vrms Exc, 1 kHz - 5 kHz Freq |
| | AC3 | 2 Ch. 28-115 Vrms (HV), 47 Hz - 2.5 kHz (max. range) | | | SD3 | 4 Ch. 2-28 Vrms Input, 2-115 Vrms Exc, 5 kHz - 10 kHz Freq |
| Thermocouple (Measure) | TC1 | 8 Ch. Thermocouple, J, K, T, E, N, B, R, S, and Low-voltage A/D | | | SD4 | 4 Ch. 2-28 Vrms Input, 2-115 Vrms Exc, 10 kHz - 20 kHz Freq |
| | TR1 | 8 Ch. RTD (RT1-type) or Thermocouple (TC1-type), programmable per Ch. | | | SD5 | 4 Ch. 28-90 Vrms Input, 2-115 Vrms Exc, 47 Hz - 1 kHz Freq |
| | RT1 | 8 Ch. RTD (2,3 or 4 wire), standard PT-type to 4 kohm | | | | |
| GPS | GP1 | Multi-Cl- (astallita) CDC 0 IDIC Dessition of Course | | | | 4 Ch. 2-28 Vrms Input, 2-115 Vrms Exc |
| | | Multi-Ch. (satellite) GPS & IRIG Receiver or Source; | | L(R)VDT-to-Dig | LD1-5 | (47 Hz - 20 kHz Freq. and 2-90 Vrms ranges, reference detailed |
| | | 2x wide module, Javad TR2 high-performance GPS engine | | | | specifications) |
| | GP2 | Multi-Ch. (satellite) GPS & IRIG Receiver or Source; 1x wide module, uBlox Neo GPS engine | | Dig-to-SYN/RSL Dig-to-L(R)VDT | DSx / DRx | 3, 2 or 1 Ch. @ 0.5 VA, 2.2 VA or 3.0 VA |
| | | | | | DLX DLX | 2-90 Vrms / 2-115 Vexc @ 47 Hz – 20 kHz |
| | | | | | DLX | (Multi-range inputs/frequency; reference module detailed specifications) |
| IRIG | RG1 | 1 Ch. IRIG Receiver or Source, digital & analog w/ master timer | 1 | Chip Detect | CD1 | Six (6) chip detection and burn channels |
| Strain Gauge | SG1 | 4 Ch. Strain Gauge, full-bridge measurement | | Variable Reluctance | VR1 | 8 Channels, Differential Input |



68ARM2 3U OpenVPX SBC

Select up to 3 functions for your application (Continued)

For a full listing of available smart functions and detailed specifications please visit https://www.naii.com/functions

| Communication | | | | | | | | | | |
|-------------------------|----------|---|--|----------|--------|--|--|--|--|--|
| Function | Module | Description | | Function | Module | Description | | | | |
| ARINC | AR1 | 12 Ch. ARINC 429/575, TX or RX | | CANBus | CB1 | 8 Ch. CAN bus, CAN 2.0 A/B Protocol | | | | |
| | AR2 | 1 Ch. ARINC 568 (TX & RX) & 1 Ch. ARINC 579 (TX or RX) | | | CB2 | 8 Ch. CAN bus, J1939 Protocol | | | | |
| | FTA, | 1, 2 & 4 Ch. MIL-STD-1553, Dual Redundant | | | | 8 Ch. CAN bus, CAN 2.0 A/B Protocol or J1939 Protocol, programmable | | | | |
| MIL-STD-1553 | FTB, FTC | XFMR-Coupled Assisted Mode Capable | | | CB3 | | | | | |
| | FTD, | 1, 2 & 4 Ch. MIL-STD-1553, Dual Redundant | | Serial | | | | | | |
| | FTE, FTF | Direct-Coupled Assisted Mode Capable | | | SC1 | 4 Ch. Serial Communications, multi-mode | | | | |
| MIL-STD-1760 | FTJ | 1 Ch. MIL-STD-1553/1760, XFMR-Coupled | | | | RS-232/422/485/423 capable, ASYNC/SYNC (S/HDLC) non-isolated | | | | |
| | FTK | 2 Ch. MIL-STD-1553/1760 XFMR-Coupled | | | SC2 | 4 Ch. Serial Communications, multi-mode programmable, isolated | | | | |
| | EM1 | 2-Port 10/100/1000Base-T Ethernet NIC, Intel 82850, | | | 563 | 8 Ch. Serial Communications RS-232/422/485 or GPIO, non-isolated | | | | |
| Ethernet | | PCIe I/F to processor (local or off-board host) | | | SC3 | | | | | |
| | | 16-Port 10/100/1000Base-T, managed switch, with L2/L3 Layer support | | | | 4 Ch. Serial Communications, multi-mode, individual GNDs, non-isolated | | | | |
| | ES2 | 4x 10Gb Fiber Optic option, 2x wide module | | | SC7 | | | | | |
| Combination & Specialty | | | | | | | | | | |
| Function | Module | Description | | Function | Module | Description | | | | |
| | CM5 | 2 Ch. MIL-STD-1553 & 8 Ch. ARINC 429/575 | | Flash | FM1 | 240 GB SSD, SATA II, MLC, -40° C to +85° C | | | | |
| | CM8 | 2 Ch. MIL-STD-1553 & 12 Ch. Discrete I/O | | | FM2 | 480 GB SSD, SATA II, MLC, -40° C to +85° C | | | | |
| | | | | | FM4 | 128 GB SSD, SATA II, SLC, -40° C to +85° C | | | | |
| Combination | | | | | FM5 | 256 GB SSD, SATA II, SLC, -40° C to +85° C | | | | |
| | | | | | FM7 | 1 TB SSD, SATA II, TLC, 0° C to +70° C | | | | |
| | | | | | FM8 | 1 TB SSD, SATA II, TLC, -40° C to +85° C | | | | |
| | | | | | FM9 | 2 TB SSD, SATA II, TLC, -40° C to +85° C | | | | |

Architected for Versatility

NAI's Configurable Open System Architecture™ (COSA®) offers a choice of over 70 smart I/O, communications, or Ethernet switch functions, providing the highest packaging density and greatest flexibility of any 3U SBC in the industry. Preexisting, fully-tested functions can be combined in an unlimited number of ways quickly and easily.

Board Support Package and Software Support

The 68ARM2 includes BSP and SDK support for Xilinx PetaLinux or Wind River® VxWorks®. Please contact the factory regarding other OS support (e.g. DDC-I Deos, etc.). In addition, software support kits are supplied, with source code and board-specific library I/O APIs, to facilitate system integration. Each I/O function has dedicated processing, unburdening the SBC from unnecessary data management overhead.

Background Built-In-Test (BIT)

BIT continuously monitors the status of all I/O during normal operations and is totally transparent to the user. SBC resources are not consumed while executing BIT routines. This simplifies maintenance, assures operational readiness, reduces life-cycle costs and - keeps your systems mission ready.

One-Source Efficiencies

Eliminate man-months of integration with a configured, field-proven system from NAI. Specification to deployment is a seamless experience as all design, state-of-the-art manufacturing, assembly and test are performed - by one trusted source. All facilities are located within the U.S. and optimized for high-mix/low volume production runs and extended lifecycle support.

Product Lifecycle Management

From design to production and beyond, NAI's product lifecycle management strategy ensures the long-term availability of COTS products through configuration management, technology refresh and obsolescence component purchase and storage



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